What is claimed is:

1. An electronic parts packaging structure, comprising:

a wiring substrate including a predetermined wiring pattern;

an electronic parts, a connection terminal on an element forming surface of which is flip-chip connected to the wiring pattern;

an insulating film for covering the electronic parts;

a via hole formed in a predetermined portion of the electronic parts and the insulating film on the connection terminal; and

an overlying wiring pattern formed on the insulating film and connected to the connection terminal via the via hole.

2. An electronic parts packaging structure, according to claim 1, wherein a side surface of the via hole formed in the electronic parts and the insulating film constitutes a continued identical surface.

3. An electronic parts packaging structure comprising:

a wiring substrate including a predetermined wiring pattern;

an electronic parts, a connection terminal on an element forming surface of which is flip-chip

connected to the wiring pattern, and the electronic parts having a through electrode which is connected to the connection terminal via a first via hole formed in the electronic parts, on a back surface;

an insulating film for covering the electronic parts;

a second via hole formed in a predetermined portion of the insulating film on the through electrode; and

an overlying wiring pattern formed on the insulating film and connected to the through electrode via the second via hole.

4. An electronic parts packaging structure, according to claim 1, wherein a side surface of the via hole formed in the electronic parts except a bottom portion is covered with an inorganic insulating film.

5. An electronic parts packaging structure, according to claim 1, wherein the electronic parts is a semiconductor chip whose thickness is about 150 μm or less.

6. An electronic parts packaging structure, according to claim 1, wherein a same structural body as the electronic parts, the insulating film, and the overlying wiring pattern, which are formed on the wiring pattern of the wiring substrate, is repeated n times (n is an integer of 1 or more) on

the overlying wiring pattern in a multi-layered fashion, and a plurality of electronic parts are connected mutually via the via hole.

7. An electronic parts packaging structure, according to claim 1, wherein a connection terminal of an overlying electronic parts is flip-chip connected to the overlying wiring pattern.

8. A method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip connecting a connection terminal of an electronic parts having the connection terminal on an element forming surface to a wiring pattern formed on or over a base substrate;

forming an insulating film for covering the electronic parts;

forming a via hole having a depth that reaches the connection terminal by etching a predetermined portion from an upper surface of the insulating film to the element forming surface of the electronic parts; and

forming an overlying wiring pattern, which is connected to the connection terminal via the via hole, on the insulating film.

9. A method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip connecting a connection terminal of an electronic parts, which has the connection

terminal on an element forming surface and has a through electrode connected to the connection terminal via a first via hole on a back surface, to a wiring pattern formed on or over a wiring substrate;

forming an insulating film for covering the electronic parts;

forming a second via hole having a depth that reaches the through electrode, by etching a predetermined portion of the insulating film on the through electrode; and

forming an overlying wiring pattern, which is connected to the through electrode via the second via hole, on the insulating film.

10. A method of manufacturing an electronic parts packaging structure, according to claim 8, wherein, in the step of forming the via hole, the insulating film and the electronic parts are etched by RIE or a laser.

11. A method of manufacturing an electronic parts packaging structure, according to claim 8, wherein the step of forming the overlying wiring pattern includes the steps of,

forming a resist film having an opening portion in a predetermined portion containing the via hole on the insulating film,

forming a conductive film pattern in the

via hole and the opening portion of the resist film, by applying a plating upward from the connection terminal exposed from a bottom portion of the via hole by means of electroplating that utilizes the wiring pattern and the connection terminal of the electronic parts connected to the wiring pattern as a plating power-supply layer, and

removing the resist film to get the overlying wiring pattern.

12. A method of manufacturing an electronic parts packaging structure, according to claim 8, after the step of forming the via hole but before the step of forming the overlying wiring pattern, further comprising the steps of:

forming an inorganic insulating film on an inner surface of the via hole and on the insulating film; and

removing the inorganic insulating film from a bottom portion of the via hole to expose the connection terminal on the bottom portion of the via hole.

13. A method of manufacturing an electronic parts packaging structure, according to claim 8, wherein a structure in which a plurality of electronic parts are stacked three- dimensionally in a multi-layered fashion and are connected mutually via the via hole is formed by repeating n times (n

is an integer of 1 or more) respective steps from the step of flip-chip connecting the electronic parts to the wiring pattern to the step of forming the overlying wiring pattern.

14. A method of manufacturing an electronic parts packaging structure, according to claim 8, after the step of forming the overlying wiring pattern, further comprising the step of:

flip-chip connecting a connection terminal of an overlying electronic parts having the connection terminal to the overlying wiring pattern.

15. A method of manufacturing an electronic parts packaging structure, according to claim 8, wherein the electronic parts is a semiconductor chip whose thickness is about 150 μm or less.